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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,355	02/28/2002	Michiaki Sakamoto	8018-1003	5587
466	7590	12/02/2004	EXAMINER WANG, GEORGE Y	
YOUNG & THOMPSON 745 SOUTH 23RD STREET 2ND FLOOR ARLINGTON, VA 22202			ART UNIT 2871	PAPER NUMBER

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/084,355

Applicant(s)

SAKAMOTO ET AL.

Examiner

George Y. Wang

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-4, 10-16, 18-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tagusa et al. (U.S. Patent No. 5,946,065, hereinafter, "Tagusa") in view of Seo et al. (U.S. Patent No. 6,445,435, hereinafter "Seo") and Applicant's Admission of Prior Art (AAPA).

1. As to claim 1, 15-16, and 22, Tagusa discloses a liquid crystal display (LCD) having a plurality of gate lines (fig. 1, ref. 22) that are parallel to each other, a plurality of data lines (fig. 1, ref. 23) that are parallel to each other and perpendicular to the gate lines, switching elements (fig. 1, ref. 24) positioned near the intersections of the gate and data lines, a plurality of pixel electrodes (fig. 1, ref. 21) over the gate and data lines with gaps (fig. 2, ref. 712) via an interlayer insulation film (fig. 2, ref. 38) between the pixel electrodes that at least partially overlap with a gate line where the source and drain electrodes overlap with the gate line to form the switching element being entirely outside the gap between adjacent pixel electrodes (fig. 1, ref. 24; col. 10, lines 31-50), and a plurality of control electrodes (fig. 1, ref. 25).

However, the reference fails to specifically disclose an LCD with an opposing active matrix substrate with a liquid crystal layer disposed between the matrix substrates and control electrodes each disposed in the gap between adjacent pixel electrodes and cover the gate line.

AAPA discloses an LCD with an opposing active matrix substrate (fig. 10, ref. 64) with a liquid crystal layer (fig. 10, ref. 65) disposed between the matrix substrates.

Seo discloses an LCD where each control electrode are disposed above the gate line between adjacent pixel regions (fig. 2a, 2b, ref. 125).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose an opposing active matrix substrate, and liquid crystal layer since one would not only recognize these elements as well known in the LCD art but also be motivated to improve the aperture ratio of the display, minimize disturbance

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in the orientation of the liquid crystal molecules, and simplify the fabrication process (Tagusa, col. 7, lines 16-21). Furthermore, the influence of the capacitance between the pixel electrodes and the lines appearing on the display, such as crosstalk, can be reduced to achieve a good display (col. 7, lines 21-24). Lastly, enhancement to brightness and wider viewing angle are also advantages (col. 7, lines 25-28).

It would have also been obvious to one of ordinary skill in the art at the time the invention was made to have disposed each control electrode between adjacent pixel regions and to directly overlie the gate line since one would be motivated to effectively create a capacitor (col. 5, lines 1-9) that ultimately yields an LCD with a high aperture ratio (col. 2, lines 15-19).

2. Regarding claims 2-4, and 21, Tagusa discloses the LCD apparatus as recited above with a control electrode that overlaps with the gap in the width direction, in the region where the gate line and pixel electrode overlap (fig. 2, 13).

3. As to claim 10, Tagusa discloses the LCD device as recited above where the interlayer insulating film comprises an organic film (fig. 2, ref. 38; col. 10, ref. 1-4).

4. Regarding claims 11-12, Tagusa, Seo, and AAPA disclose the LCD device as recited above, however, the references fail to specifically disclose the LCD having a COT structure or a reflection type LCD.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a reflection type structure since one would motivated to eliminate the need for back light and ultimately reduce power consumption (col. 1, lines 19-25). In addition, it would have been obvious to one of ordinary skill in the art to have equally used because Applicant has failed to address any particular advantage of such a structure and because a COT structure is functionally equivalent to a reflection type LCD and serves the same purpose.

5. Regarding claims 13-14 and 18-19, Tagusa disclose the LCD device as recited above where the control and source electrode are coupled via an extension to the contact hole (fig. 1, ref. 26) to the pixel electrode.

6. Claims 5-9, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tagusa, Seo, and AAPA in view of Yao et al. (U.S. Patent No. 5,682,211, from hereinafter, "Yao").

Tagusa discloses the LCD device as recited above, however, the references fail to specifically disclose a control electrode having the same potential voltage as that of the source electrode of the switching element. Furthermore, the references fail to specifically teach the control electrode on the same layer and integrally formed with the source electrode, having a multilayer structure comprising of metal.

Yao discloses an LCD device with a control electrode having the same potential voltage as that of the source electrode of the switching element (col. 3, lines 56-67).

Furthermore, Yao teaches the control electrode on the same layer and integrally formed with the source electrode (fig. 4, ref. 25), having a multilayer structure (fig. 2, ref. 41) comprising of metal (fig. 2, ref. 66, 62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a control electrode having the same potential voltage as that of the source electrode of the switching element, the control electrode on the same layer and integrally formed with the source electrode, having a multilayer structure comprising of metal create an integral since one would be motivated to create a functioning LCD with optimized display quality and increased viewing angle (col. 2, lines 22-36).

Response to Arguments

7. Applicant's arguments filed September 7, 2004 have been fully considered but they are not persuasive.

Applicant's main argument is that the cited prior art references fail to specifically teach that "a control electrode disposed in a gap between adjacent pixel electrodes and directly overlying the gate line" (Applicant's Remarks, p. 2). Furthermore, Applicant argues that there is no motivation to combine the references based on a misunderstanding from a previous telephone call, the incompatibility of the cited references, and different inventive purposes of the references. However, Examiner disagrees.

With regard to Applicant's first argument, it appears that Applicant has misconstrued the previous telephone communication with Examiner to argue that the pixel *electrode* (as opposed to the pixel *region*) is between the gate and data layers, making it unlikely to combine the Seo reference with Tagusa. However, this is not true of the telephone conversation and not true of Seo's abstract reference. The question Applicant had asked the Examiner was regarding the pixel *region*. As a result, when Examiner pointed to the abstract of the Seo reference, Applicant was satisfied with and no further issues were apparent. Therefore, Examiner clarifies again that the reference to the abstract of the Seo reference was to show that the pixel *region* was formed and defined by the area between the gate and data lines.

With regard to Applicant's second argument pertaining to the capacitor structure of Seo and the microscopic hollows of Tagusa, Applicant asserts that a three layered structure of a common electrode over the data electrode would have to be implemented but would increase the size/thickness of Tagusa's capacitor, ultimately teaching away from the invention. However, Examiner disagrees. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Thus, there is no reason why the Seo reference, in order to be relevant, must implement a three layered structure. In fact, Applicant offers not reason but merely assumes this without any

justification. Furthermore, even if a three-layered structure were implemented, such a structure does not obviate the combination since the Seo reference is not offered to provide new structures, but rather that the control electrode can be disposed above the gate line between adjacent pixel regions.

With regard to Applicant's argument that the reference have different inventive purposes, Applicant argues that these differences offer no motivation for their combination. However, Examiner disagrees. First, it is clear that that the references are both concerned with preventing light leakage. In fact, Applicant admits this on p. 6 of his Remarks. And while Applicant goes to great length to discuss the use or nonuse of a black matrix in the reference, Examiner notes that these arguments are irrelevant since the question at hand has to do with the position of the control electrode to be above the gate line between adjacent pixel regions. As a result, the discuss on the black matrix or other structures does not obviate the combination since the Seo reference is not offered to provide new structures, but rather that the control electrode can be disposed above the gate line between adjacent pixel regions.

Therefore, Examiner holds to the validity of the references used and maintains rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 571-272-2304. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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gw
November 24, 2004



TARIFUR R. CHOWDHURY
PRIMARY EXAMINER